

FIG.1

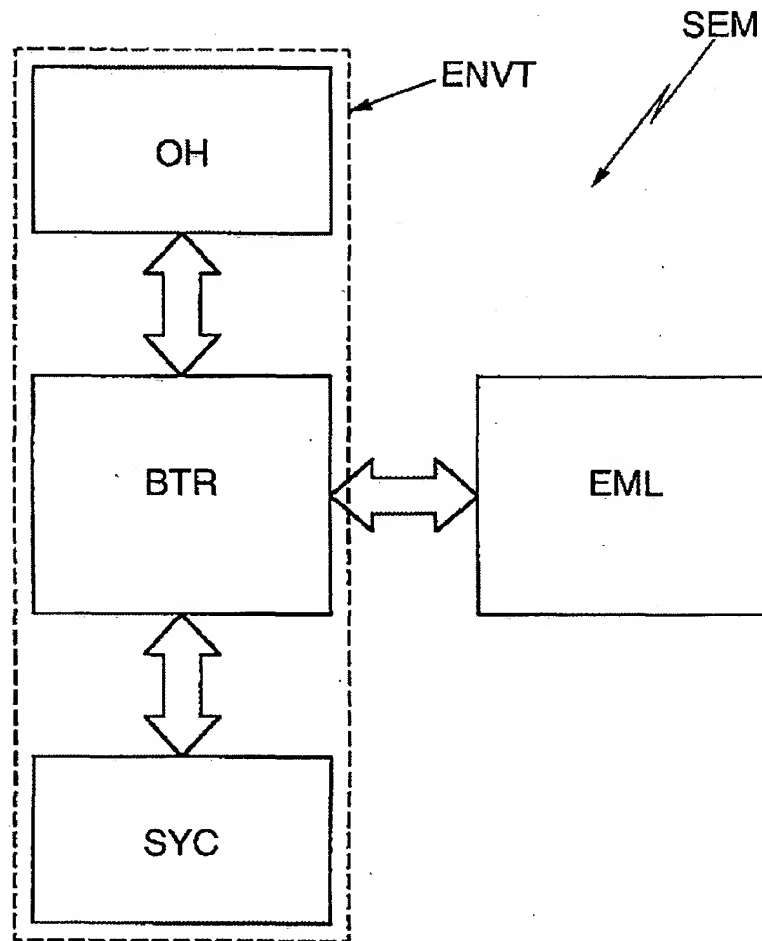


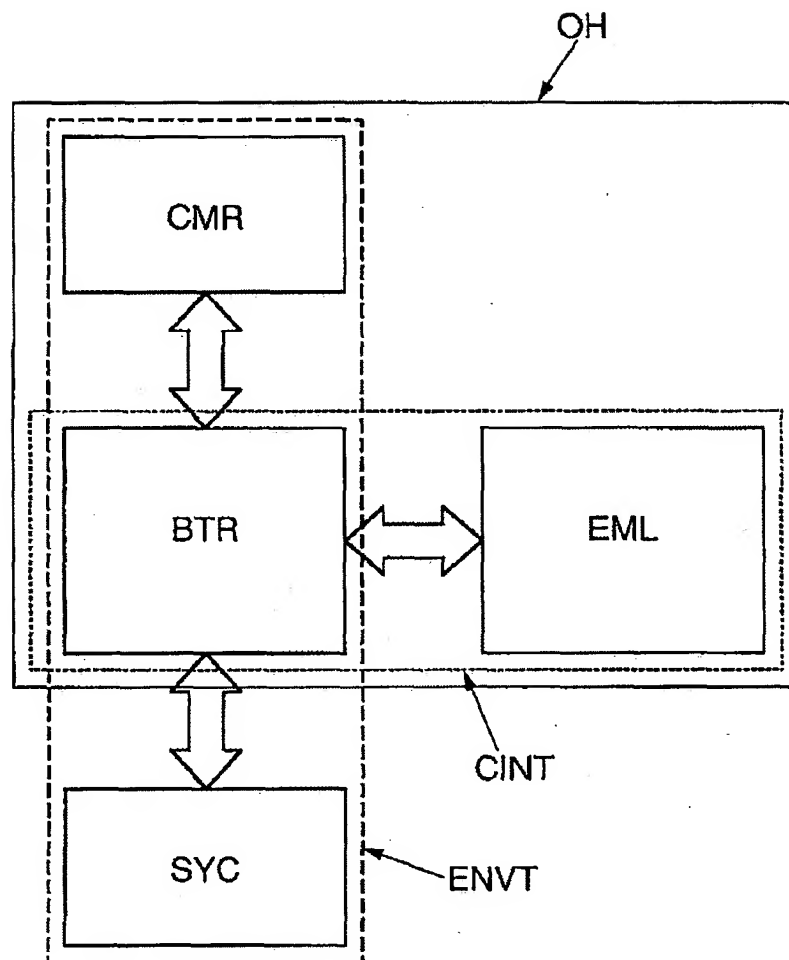
FIG.2

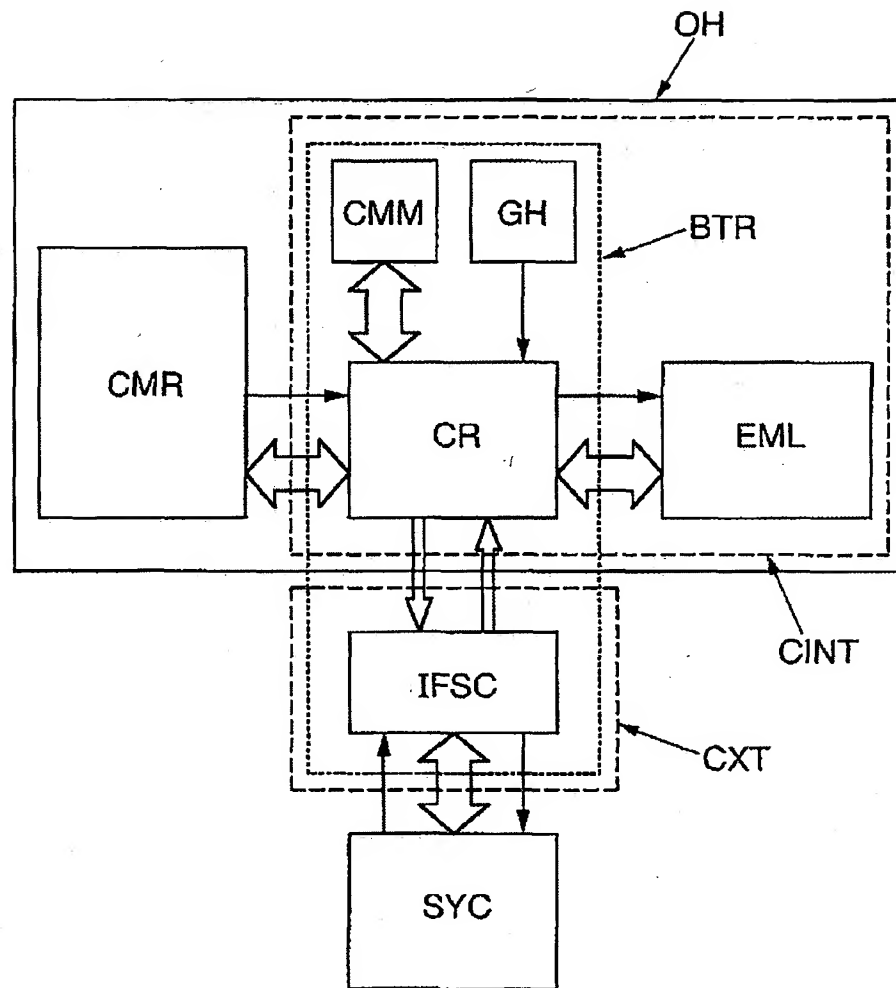
FIG.3

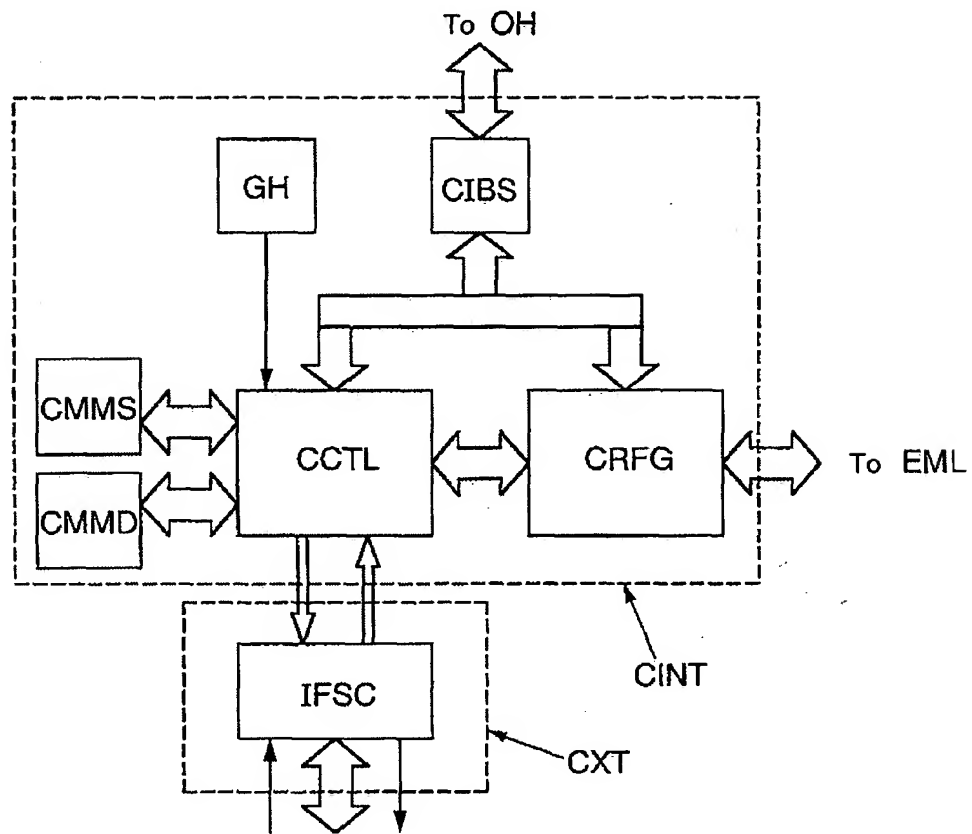
FIG.4

FIG.5

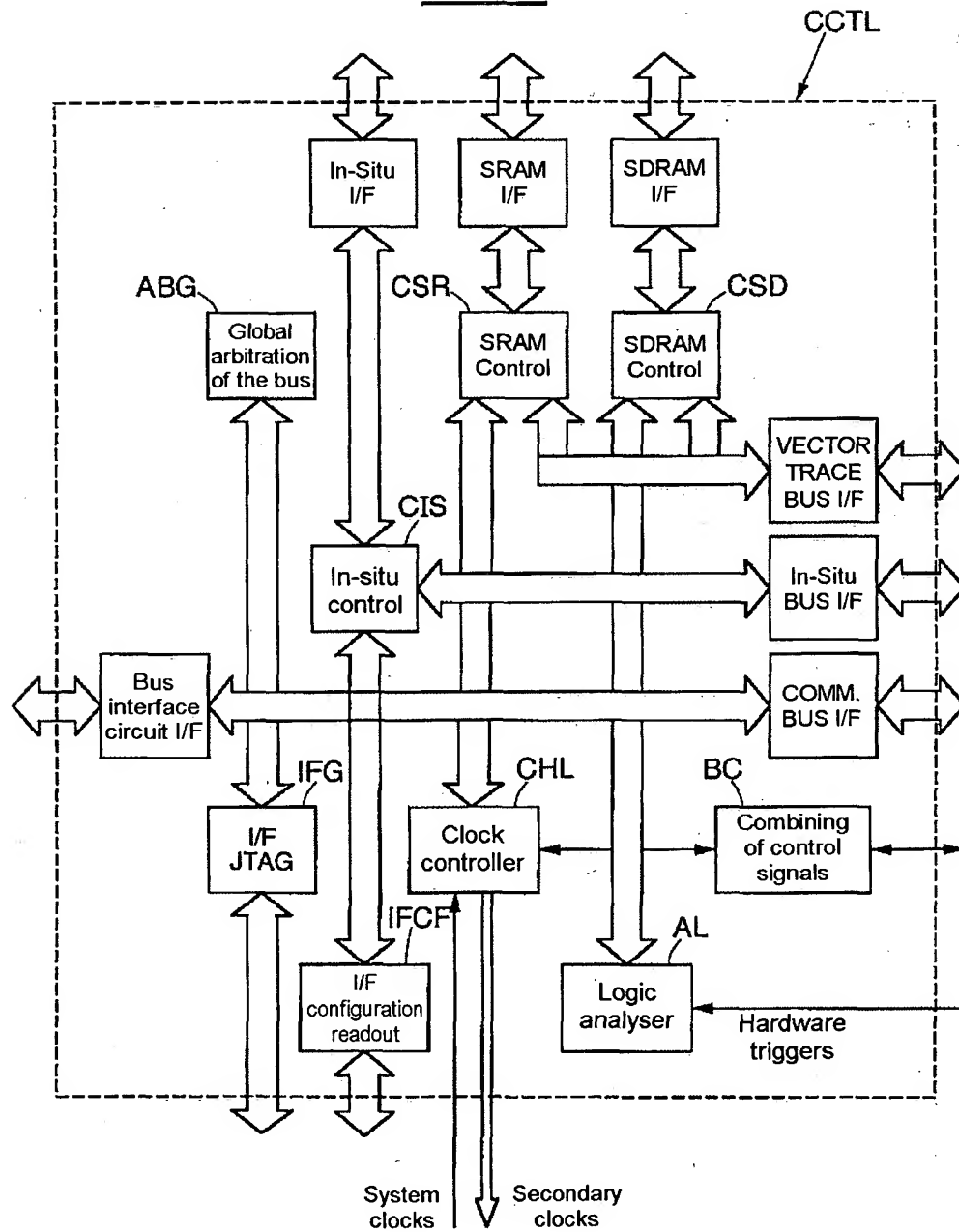


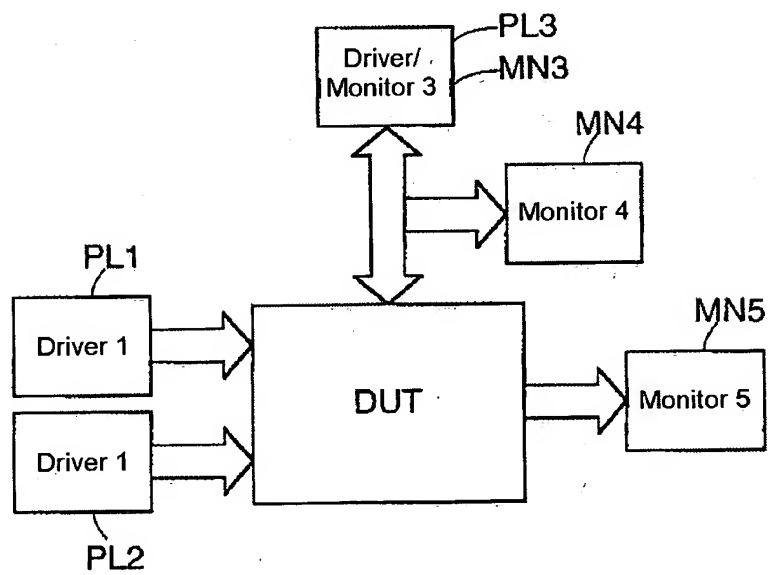
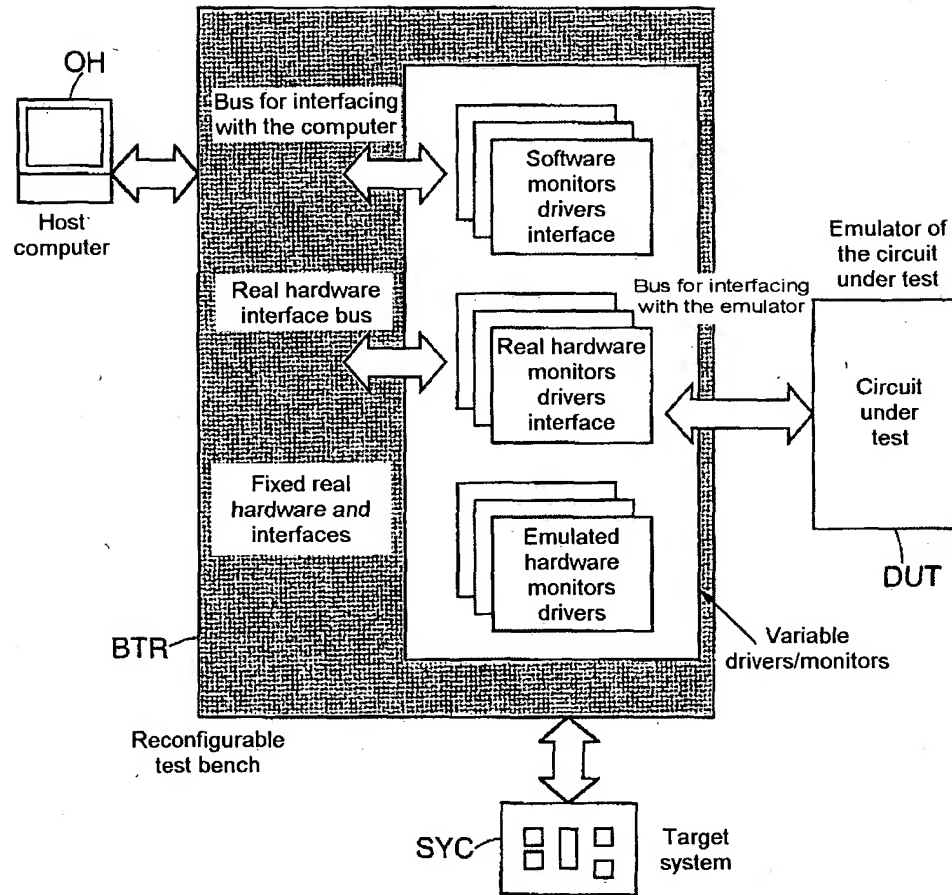
FIG.6

FIG.7a



8/14

FIG.7b

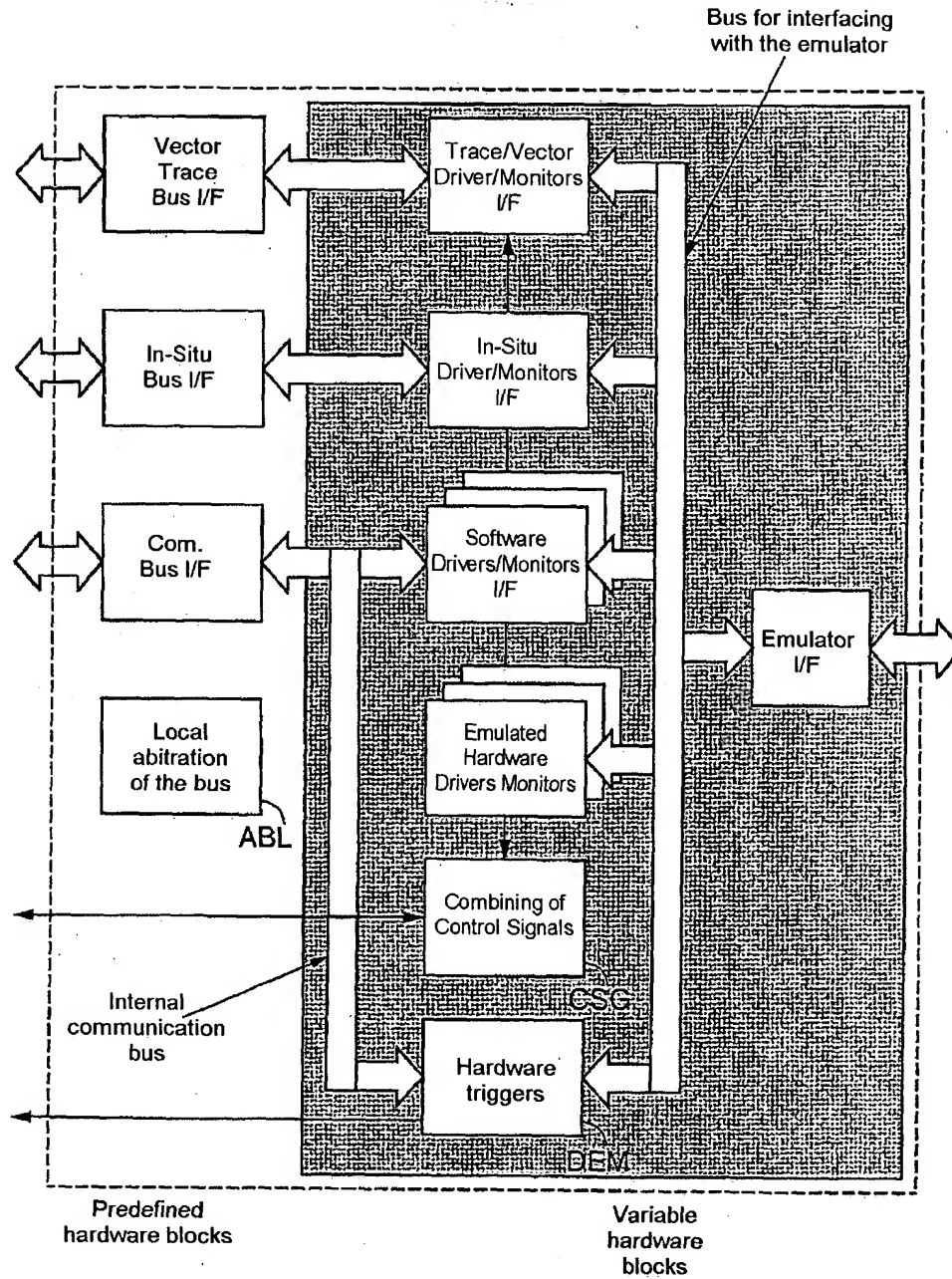


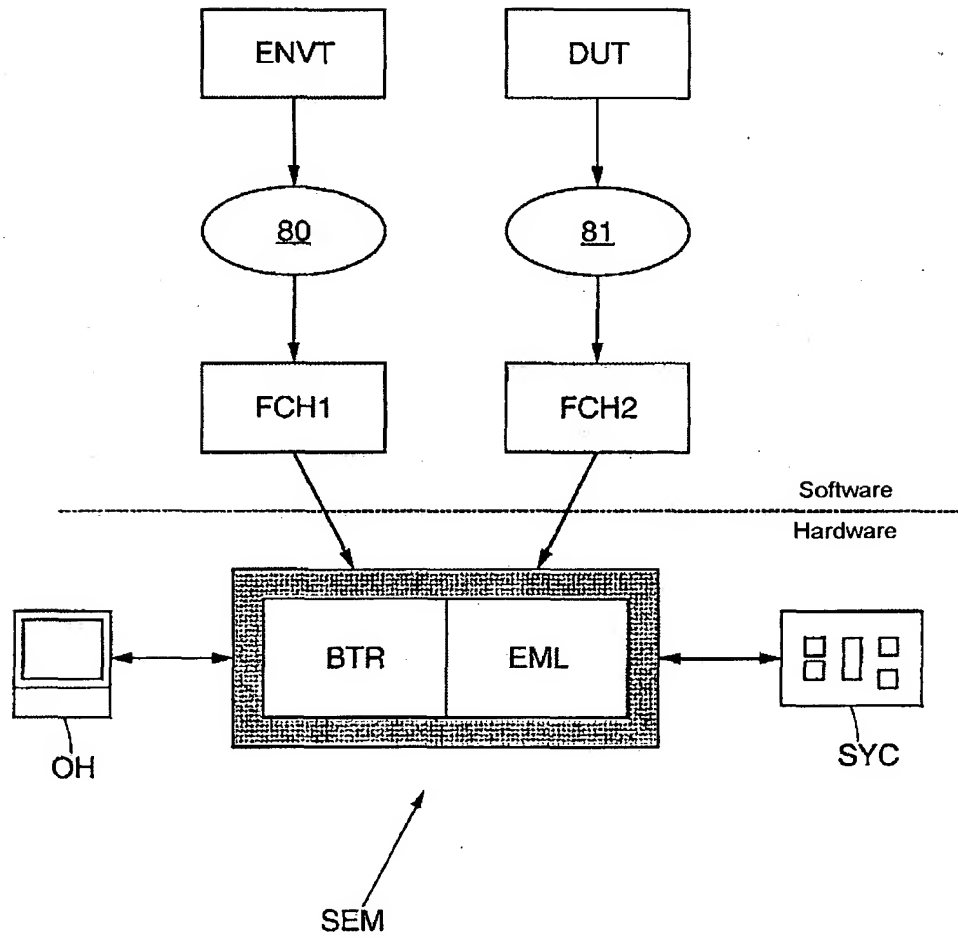
FIG.8

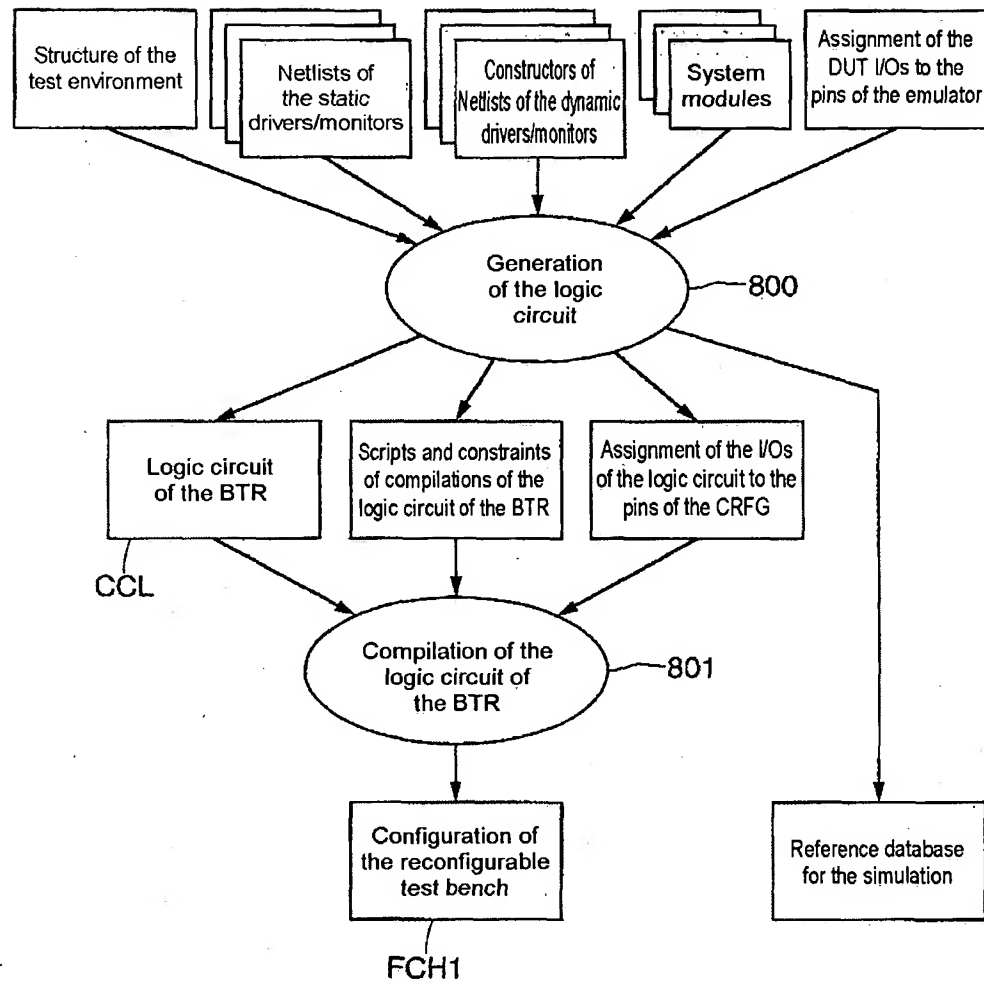
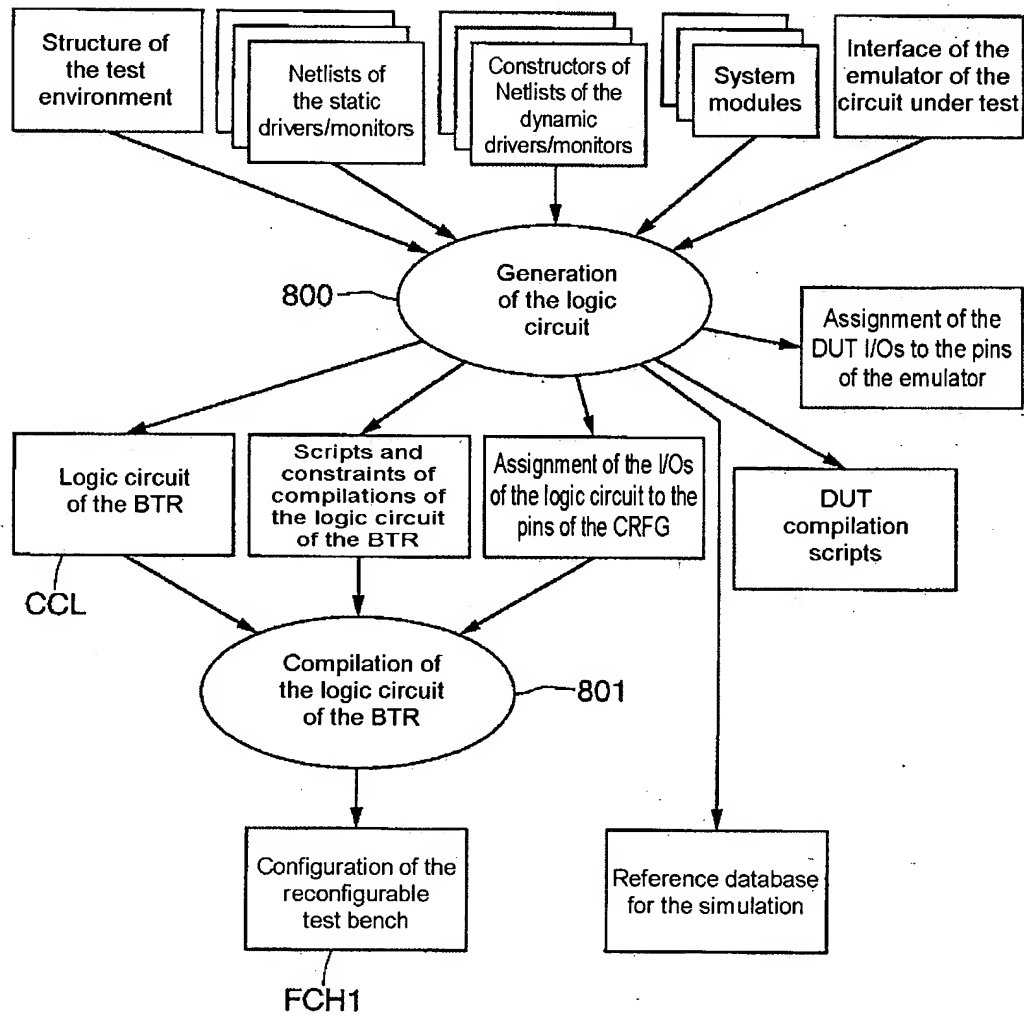
FIG. 9a

FIG.9b

12/14

FIG.10

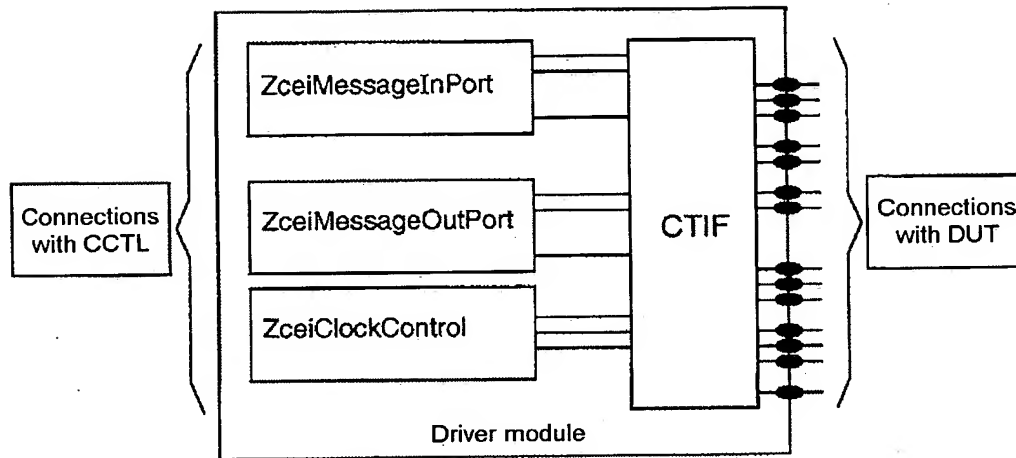


FIG.11

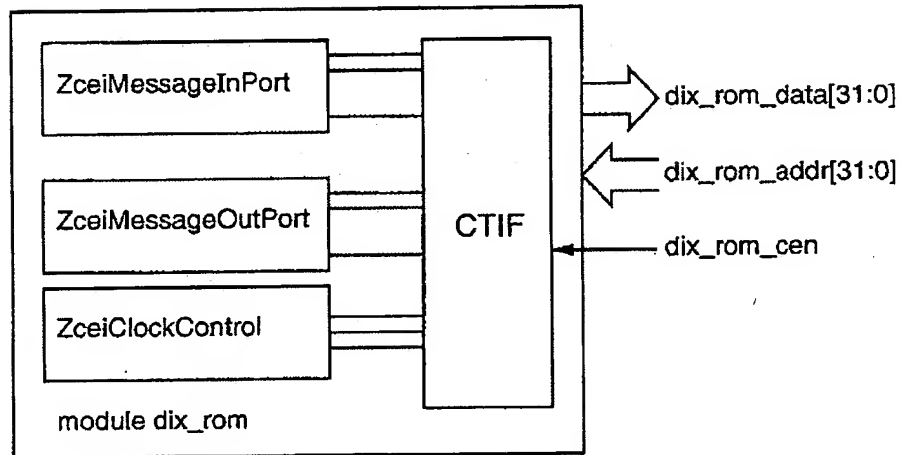


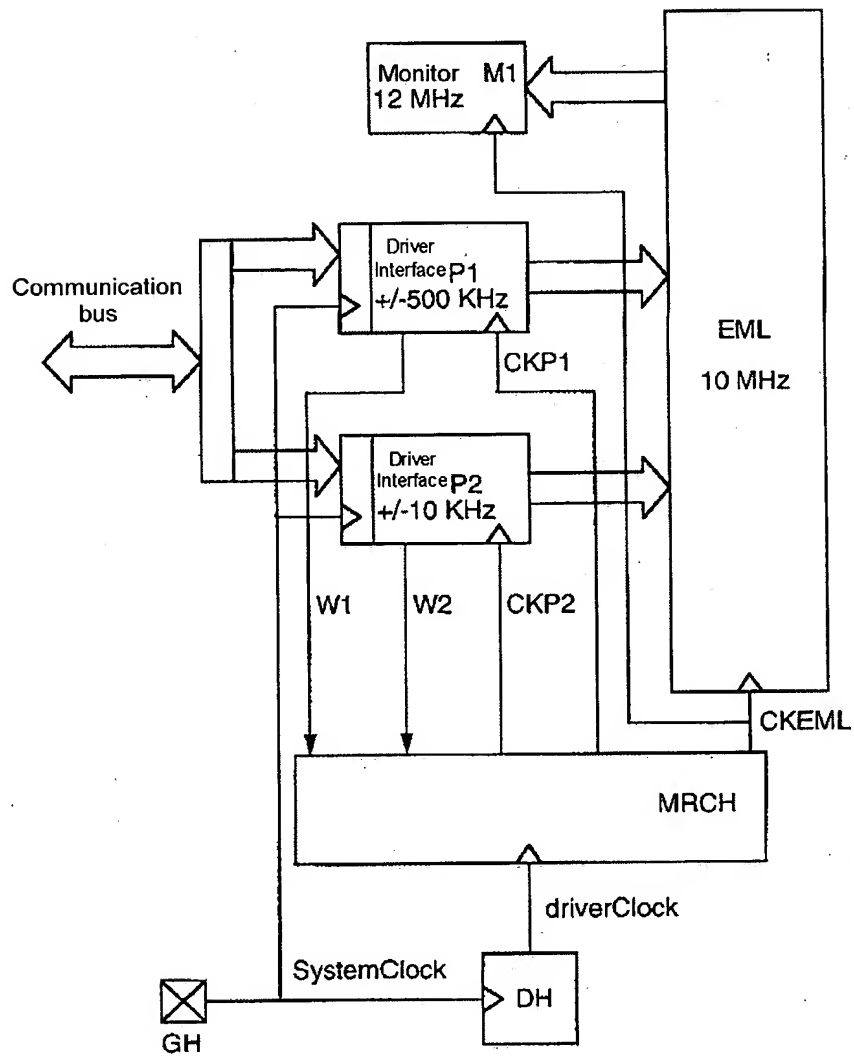
FIG.12a

FIG.12b

W1	W2	CKP1	CKP2	CKEML
0	0	DriverClock	DriverClock	DriverClock
0	1	Inactive	DriverClock	Inactive
1	0	DriverClock	Inactive	Inactive
1	1	DriverClock	DriverClock	Inactive